19-4126; Rev 0; 7/08

Dual, 12-Bit, 1.25Msps Simultaneous-Sampling ADCs with Serial Interface

General Description

The MAX1377/MAX1379/MAX1383 feature two simultaneous-sampling, low-power, 12-bit ADCs with serial interface and internal voltage reference. Fast sampling rate, low power dissipation, and excellent dynamic performance make the MAX1377/MAX1379/MAX1383 ideal for industrial process control, motor control, and RF applications.

Conversion results are available through a SPI™-/QSPI™-/MICROWIRE™-/DSP-compatible interface with independent serial digital outputs for each channel. The serial outputs allow twice as much data to be transferred at the given clock rate. The conversion results for both ADCs can also be output on a single digital output for microcontrollers (µCs) and DSPs with only a single serial input available.

The MAX1377 operates from a 2.7V to 3.6V analog supply and the MAX1379/MAX1383 operate from a 4.75V to 5.25V analog supply. A separate 1.8V to AVDD digital supply allows interfacing to low voltage logic without the use of level translators.

Two power-down modes, partial and full, allow the MAX1377/MAX1379 and MAX1383 (full power-down only) to save power between conversions. Partial power-down mode reduces the supply current to 2mA while leaving the reference enabled for quick power-up. Full power-down mode reduces the supply current to 1µA.

The MAX1377/MAX1379 inputs accept voltages between zero and the reference voltage or ±V_{REF}/2. The MAX1383 offers an input voltage range of ±10V, which is ideal for industrial and motor-control applications. The input to each of the ADCs supports either a true-differential input or two single-ended inputs.

The MAX1377/MAX1379/MAX1383 are available in a 20-pin TQFN package, and are specified for the automotive (-40°C to +125°C) temperature range.

Applications

Motor Control

Communications

Data Acquisition

Bill Validation

Portable Instruments

SPI/QSPI are trademarks of Motorola, Inc.

MICROWIRE is a trademark of National Semiconductor Corp.

Features

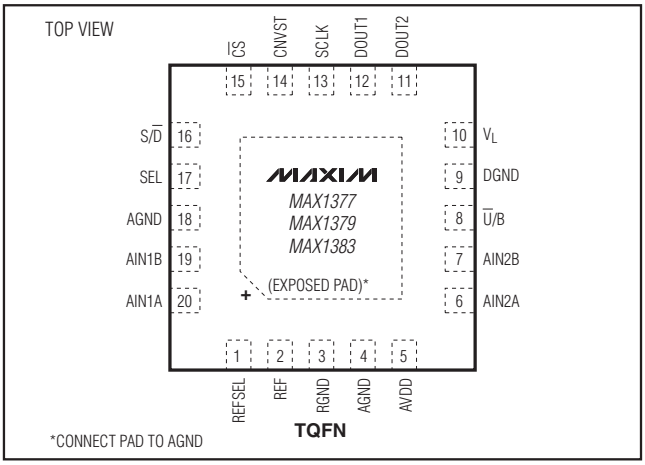
- **Dual, Simultaneous-Sampling, 12-Bit Successive Approximation Register (SAR) ADCs**
- **2 x 2 Mux Inputs or Two Differential Inputs**
- **1.25Msps Sampling Rate per ADC**
- **Internal or External Reference**
- **Excellent Dynamic Performance**
  - **70dB SINAD (MAX1377)**
  - **71dB SINAD (MAX1379/MAX1383)**
  - **84dBc/SFDR**
  - **1MHz Full-Linear Bandwidth**
- **2.7V to 3.6V Low-Power Operation (MAX1377)**
  - **50mW (Normal Operation)**
  - **6mW (Partial Power-Down)**
  - **3µW (Full Power-Down)**
- **4.75V to 5.25V Low-Power Operation (MAX1379)**
  - **90mW (Normal Operation)**
  - **10mW (Partial Power-Down)**
  - **5µW (Full Power-Down)**
- **20MHz, SPI-Compatible, 3-Wire Serial Interface**
  User-Selectable Single (0.625Msps max) or Dual Outputs (1.25Msps max)
- **Input Range: ±10V (MAX1383), 0–V_{REF} or ±V_{REF}/2 (MAX1377/MAX1379)**
- **Small 20-Pin TQFN Package**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX1377ATP+	-40°C to +125°C	20 TQFN-EP*
MAX1379ATP+	-40°C to +125°C	20 TQFN-EP*
MAX1383ATP+**	-40°C to +125°C	20 TQFN-EP*

+Denotes a lead-free/RoHS-compliant package.
**EP = Exposed pad.*
***Future product—contact factory for availability.*

Pin Configuration



Dual, 12-Bit, 1.25Msps Simultaneous-Sampling ADCs with Serial Interface

ABSOLUTE MAXIMUM RATINGS

AVDD to AGND .....-0.3V to +6V
V_L to DGND .....-0.3V to +6V
SCLK, $\overline{CS}$, CNVST, $\overline{U}$/B, S/$\overline{D}$, SEL,
REFSEL to DGND.....-0.3V to (V_L + 0.3V)
DOUT_ to DGND.....-0.3V to (V_L + 0.3V)
AIN1A, AIN1B, AIN2A, AIN2B to AGND
MAX1377/MAX1379 .....-0.3V to (AVDD + 0.3V)
MAX1383.....-12V to +12V
RGND to AGND.....-0.3V to +0.3V
RGND to DGND.....-0.3V to +0.3V
DGND to AGND.....-0.3V to +0.3V
Maximum Current into Any Pin (except power-supply pins).....50mA
Continuous Power Dissipation (T_A = +70°C)
20-Pin Thin QFN (derate 34.5mW/°C above +70°C) ...2758.6mW
Operating Temperature Range .....-40°C to +125°C
Junction Temperature.....+150°C
Storage Temperature Range .....-60°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—MAX1377

(V_{AVDD} = 2.7V to 3.6V, V_L = 1.8V to AVDD, f_{SCLK} = 20MHz (50% duty cycle), V_{REF} = 2.048V, REFSEL = V_L, S/$\overline{D}$ = DGND, C_{REF} = 1µF; T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY						
Resolution			12			Bits
Relative Accuracy	INL	(Note 1)	-1.25		+1.25	LSB
Differential Nonlinearity	DNL		-1		+1.5	LSB
Offset Error					±8	LSB
Offset-Error Matching					±12	LSB
Gain Error		(Note 2)			±6	LSB
Gain-Error Matching		(Note 2)			±6	LSB
Gain Temperature Coefficient				±2		ppm/°C
DC Input Isolation		AIN1A to AIN1B, AIN2A to AIN2B		80		dB
		AIN1A to AIN2A, AIN1B to AIN2B		80		
DYNAMIC SPECIFICATIONS (f_{IN} = 500kHz, 2V_{P-P} sine wave, 1.25Msps, 20MHz f_{SCLK})						
Signal-to-Noise Plus Distortion	SINAD	Unipolar	66	69.5		dB
		Bipolar	67	70		
Signal-to-Noise Ratio	SNR	Unipolar	66	70		dB
		Bipolar	67	70		
Total Harmonic Distortion	THD	Up to the 5th harmonic		-84	-74	dB
Spurious-Free Dynamic Range	SFDR			-86	-76	dB
Intermodulation Distortion	IMD	f_{IN1} = 103.5kHz, f_{IN2} = 113.5kHz		-78		dB
Full-Power Bandwidth		-3dB point		5		MHz
Full-Linear Bandwidth		(S/N + D) > 68dB, 1V input		1		MHz
CONVERSION RATE (Figure 4)						
Minimum Conversion Time	t_{CONV}	16 clock cycles per conversion (Note 3)			0.800	µs
Maximum Throughput Rate		Dual output mode, S/$\overline{D}$ = 0	1.25			Msps
		Single output mode, S/$\overline{D}$ = 1	0.625			
Minimum Throughput Rate for Full Bandwidth Signal		(Note 4)	10			ksps

ELECTRICAL CHARACTERISTICS—MAX1377 (continued)

(V_{AVDD} = 2.7V to 3.6V, V_L = 1.8V to AVDD, f_{SCLK} = 20MHz (50% duty cycle), V_{REF} = 2.048V, REFSEL = V_L, S/$\overline{D}$ = DGND, C_{REF} = 1µF; T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Track-and-Hold Acquisition Time	t_{ACQ}			125		ns
Aperture Delay				2		ns
Aperture-Delay Matching				2		ns
Aperture Jitter		(Note 5)		30		ps
External Clock Frequency	f_{SCLK}				20	MHz
ANALOG INPUTS (AIN1A, AIN1B, AIN2A, AIN2B)						
Input Range		$\overline{U}$/B = 0, V_{AIN_A} - RGND	0		V_{REF}	V
Differential Input Range		$\overline{U}$/B = 1, V_{AIN_A} - V_{AIN_B}	-V_{REF}/2		+V_{REF}/2	V
Absolute Voltage Range			0		AVDD	V
DC Leakage Current					±1	µA
Input Impedance				34		kΩ
Input Capacitance		At each analog input		16		pF
EXTERNAL REFERENCE (REFSEL = 1)						
Absolute Input Voltage Range	V_{REF}		1.0		AVDD + 0.05	V
Input Capacitance				50		pF
DC Leakage Current					±1	µA
Input Current		Time averaged at maximum throughput rate		800		µA
INTERNAL REFERENCE (REFSEL = 0)						
Reference Voltage Level			2.028	2.048	2.068	V
Load Regulation		I_{SOURCE} = 0 to 1mA		1		mV/mA
		I_{SINK} = 0 to 50µA		1		
Voltage Temperature Coefficient				±50.0		ppm/°C
DIGITAL INPUTS (SCLK, CNVST, $\overline{U}$/B, S/$\overline{D}$, SEL, REFSEL)						
Input-Voltage Low	V_{IL}				0.3 x V_L	V
Input-Voltage High	V_{IH}		0.7 x V_L			V
Input Leakage Current	I_{IL}				±10	µA
DIGITAL OUTPUT (DOUT1, DOUT2)						
Output Load Capacitance	C_{DOUT}	For stated timing performance			30	pF
Output-Voltage Low	V_{OL}	I_{SINK} = 5mA			0.4	V
Output-Voltage High	V_{OH}	I_{SOURCE} = 1mA, V_L ≥ 2.7V	V_L - 0.5V			V
Output Leakage Current	I_{OL}	High-impedance mode (Figure 9)		±0.2		µA
POWER REQUIREMENTS						
Analog Supply Voltage	AVDD		2.7	3.0	3.6	V
Digital Supply Voltage	V_L		1.8		AVDD	V

Dual, 12-Bit, 1.25Msps Simultaneous-Sampling ADCs with Serial Interface

ELECTRICAL CHARACTERISTICS—MAX1377 (continued)

(V_{AVDD} = 2.7V to 3.6V, V_L = 1.8V to AVDD, f_{SCLK} = 20MHz (50% duty cycle), V_{REF} = 2.048V, REFSEL = V_L, S/$\overline{D}$ = DGND, C_{REF} = 1µF; T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Analog Supply Current	I_{AVDD}	Normal operation		13	15	mA
		Partial power-down mode (Note 5)		2		
		Full power-down mode (Note 5)		1	5	µA
Average Static Supply Current				8	10	mA
Digital Supply Current	I_{VL}	f_{SCLK} = 20MHz, V_L = 3V, C_L = 30pF		1	1.5	mA
Power-Supply Rejection	PSR	V_{AVDD} = 3V ±10%, full-scale input		±0.2	±3	mV

ELECTRICAL CHARACTERISTICS—MAX1379

(V_{AVDD} = 4.75V to 5.25V, V_L = 3V, f_{SCLK} = 20MHz (50% duty cycle), V_{REF} = 4.096V, REFSEL = V_L, S/$\overline{D}$ = DGND, C_{REF} = 1µF; T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY						
Resolution			12			Bits
Relative Accuracy	INL	(Note 1)	-1.25		+1.25	LSB
Differential Nonlinearity	DNL		-1		+1	LSB
Offset Error					±8	LSB
Offset-Error Matching					±9	LSB
Gain Error		(Note 2)			±6	LSB
Gain-Error Matching		(Note 2)			±9	LSB
Gain Temperature Coefficient				±2		ppm/°C
DC Input Isolation		AIN1A to AIN1B, AIN2A to AIN2B		80		dB
		AIN1A to AIN2A, AIN1B to AIN2B		80		
DYNAMIC SPECIFICATIONS (f_{IN} = 500kHz , 4V_{P-P} sine wave, 1.25Msps, 20MHz f_{SCLK})						
Signal-to-Noise Plus Distortion	SINAD	Unipolar	69	70		dB
		Bipolar	70	71		
Signal-to-Noise Ratio	SNR	Unipolar	70	71		dB
		Bipolar	70	72		
Total Harmonic Distortion	THD	Up to the 5th harmonic		-84	-76	dB
Spurious-Free Dynamic Range	SFDR			-84	-76	dB
Intermodulation Distortion	IMD	f_{IN1} = 103.5kHz, f_{IN2} = 113.5kHz		-78		dB
Full-Power Bandwidth		-3dB point		5		MHz
Full-Linear Bandwidth		(S/N + D) > 68dB, 1V input		1		MHz
CONVERSION RATE (Figure 6)						
Minimum Conversion Time	t_{CONV}	16 clock cycles per conversion (Note 3)			0.8	µs
Maximum Throughput Rate		Dual-output mode, S/$\overline{D}$ = 0	1.25			Msps
		Single-output mode, S/$\overline{D}$ = 1	0.625			
Minimum Throughput Rate for Full Bandwidth Signal		(Note 4)	10			ksps

ELECTRICAL CHARACTERISTICS—MAX1379 (continued)

(V_{AVDD} = 4.75V to 5.25V, V_L = 3V, f_{SCLK} = 20MHz (50% duty cycle), V_{REF} = 4.096V, REFSEL = V_L, S/$\overline{D}$ = DGND, C_{REF} = 1µF; T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Track-and-Hold Acquisition Time	t_{ACQ}			125		ns
Aperture Delay				2		ns
Aperture-Delay Matching				2		ns
Aperture Jitter		(Note 5)		30		ps
External Clock Frequency	f_{SCLK}				20	MHz
ANALOG INPUTS (AIN1A, AIN1B, AIN2A, AIN2B)						
Input Range		$\overline{U}$/B = 0, V_{AIN_A} - RGND	0		V_{REF}	V
Differential Input Range		$\overline{U}$/B = 1, V_{AIN_A} - V_{AIN_B}	-V_{REF}/2		+V_{REF}/2	V
Absolute Voltage Range			0		AVDD	V
DC Leakage Current					±1	µA
Input Impedance				34		kΩ
Input Capcitance		At each analog input		16		pF
EXTERNAL REFERENCE (REFSEL = 1)						
Absolute Input Voltage Range	V_{REF}		1.0		AVDD + 0.05	V
Input Capacitance				50		pF
DC Leakage Current					±1	µA
Input Current		Time averaged at maximum throughput rate		800		µA
INTERNAL REFERENCE (REFSEL = 0)						
Reference Voltage Level			4.086	4.096	4.106	V
Load Regulation		I_{SOURCE} = 0 to 1mA		1		mV/mA
		I_{SINK} = 0 to 50µA		1		mV/mA
Voltage Temperature Coefficient				±50.0		ppm/°C
DIGITAL INPUTS (SCLK, CNVST, $\overline{U}$/B, S/$\overline{D}$, SEL, REFSEL)						
Input-Voltage Low	V_{IL}				0.3 x V_L	V
Input-Voltage High	V_{IH}		0.7 x V_L			V
Input Leakage Current	I_{IL}				±10	µA
DIGITAL OUTPUT (DOUT1, DOUT2)						
Output Load Capacitance	C_{DOUT}	For stated timing performance			30	pF
Output-Voltage Low	V_{OL}	I_{SINK} = 5mA			0.4	V
Output-Voltage High	V_{OH}	I_{SOURCE} = 1mA, V_L ≥ 2.7V	V_L - 0.5V			V
Output Leakage Current	I_{OL}	High-impedance mode (Figure 9)		±0.2		µA
POWER REQUIREMENTS						
Analog Supply Voltage	AVDD		4.25	5.0	5.25	V
Digital Supply Voltage	V_L		1.8		AVDD	V

Dual, 12-Bit, 1.25Msps Simultaneous-Sampling ADCs with Serial Interface

ELECTRICAL CHARACTERISTICS—MAX1379 (continued)

(V_{AVDD} = 4.75V to 5.25V, V_L = 3V, f_{SCLK} = 20MHz (50% duty cycle), V_{REF} = 4.096V, REFSEL = V_L, S/$\overline{D}$ = DGND, C_{REF} = 1µF; T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Analog Supply Current	I_{AVDD}	Normal operation		16	18	mA
		Partial power-down mode (Note 5)		2		
		Full power-down mode (Note 5)			5	µA
Average Static Current				9	10	mA
Digital Supply Current	I_{VL}	f_{SCLK} = 20MHz, V_L = 5V, C_L = 30pF		2	3	mA
		f_{SCLK} = 20MHz, V_L = 3V, C_L = 30pF		1		
Power-Supply Rejection	PSR	V_{AVDD} = 5V ±10%, full-scale input		±0.2	±3	mV

TIMING CHARACTERISTICS (Figures 6, 10)

(V_{AVDD} = 4.25V to 5.25V, V_L = 1.8V to AVDD, V_{REF} = 4.096V, f_{SCLK} = 20MHz for MAX1379, 50% duty cycle, C_L = 30pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
SCLK Clock Period	t_{CP}		50			ns
SCLK Duty Cycle	t_{CH}/t_{CL}		45		55	%
SCLK Pulse-Width High	t_{CH}		22.5			ns
SCLK Pulse-Width Low	t_{CL}		22.5			ns
SCLK Rise to DOUT_ Transition	t_{DOUT}	C_L = 30pF, V_L = 5V			14	ns
		C_L = 30pF, V_L = 3V			17	
		C_L = 30pF, V_L = 1.8V			24	
DOUT_ Remains Valid After SCLK	t_{DHOLD}		4			ns
CNVST Fall to SCLK Fall	t_{SETUP}	C_L = 30pF	10			ns
CNVST Pulse Width	t_{CSW}		20			ns
Power-Up Time; Full Power-Down	t_{PWR-UP}	External load on REF < 3µF		2		ms
SEL to CNVST Fall	t_{SEL_SETUP}		100	120		ns
SEL Hold to CNVST Fall			10			ns
$\overline{CS}$ Fall To CNVST Fall	t_{CST}	External load on REF < 3µF		2		ms
Restart Time; Partial Power-Down	t_{RCV}	No external load		16		Cycles

Note 1: Relative accuracy is the deviation of the analog value at any code from its theoretical value after the gain error and the offset error have been nulled.

Note 2: Offset nulled.

Note 3: Conversion time is defined as the number of clock cycles (16) multiplied by the clock period. Clock has 50% duty cycle.

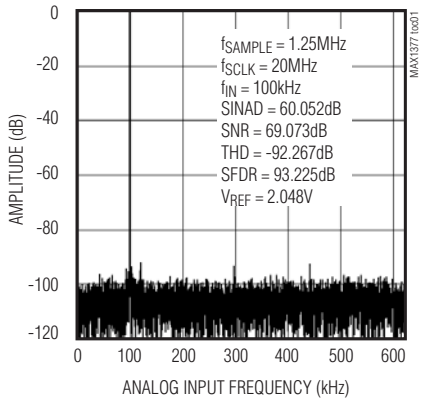
Note 4: At sample rates below 10ksps, the input full linear bandwidth is reduced to 5kHz.

Note 5: SCLK and CNVST not switching during measurement.

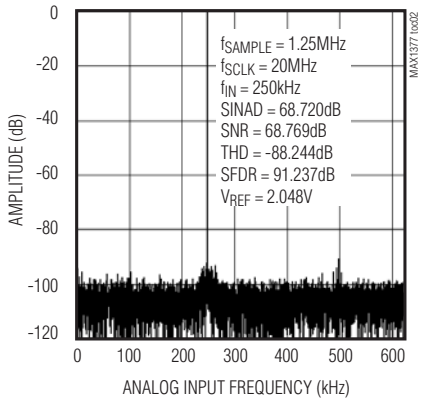
Typical Operating Characteristics

(V_{AVDD} = 5V/3V, V_L = 3V, f_{SCLK} = 20MHz, T_A = +25°C, unless otherwise noted.)

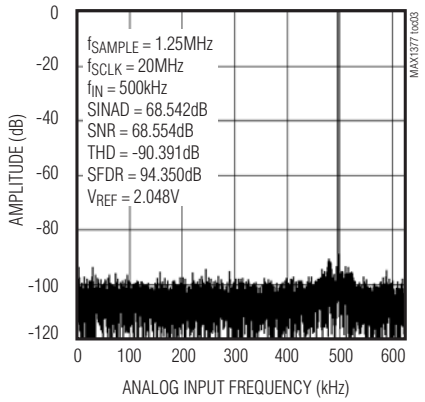
MAX1377 BIPOLAR FFT



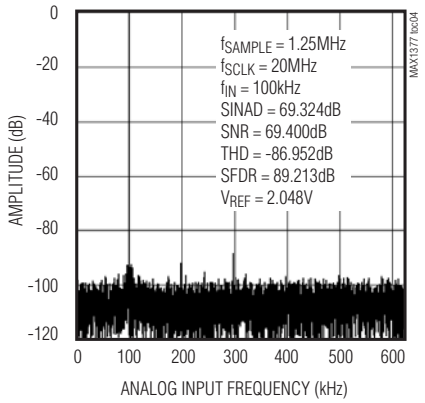
MAX1377 BIPOLAR FFT



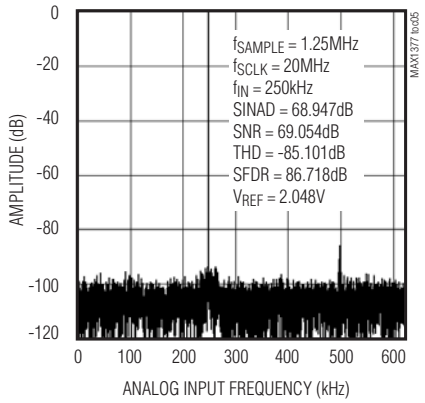
MAX1377 BIPOLAR FFT



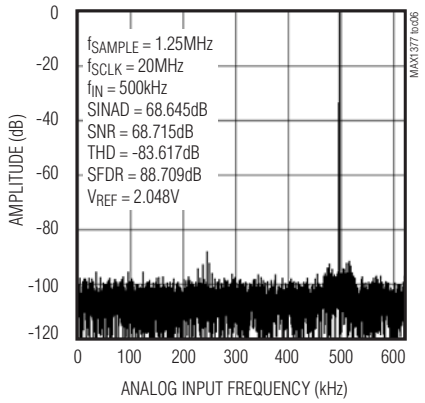
MAX1377 UNIPOLAR FFT



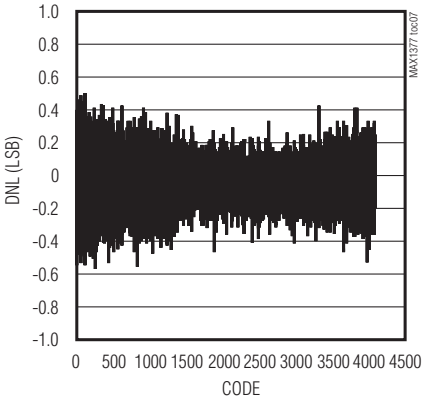
MAX1377 UNIPOLAR FFT



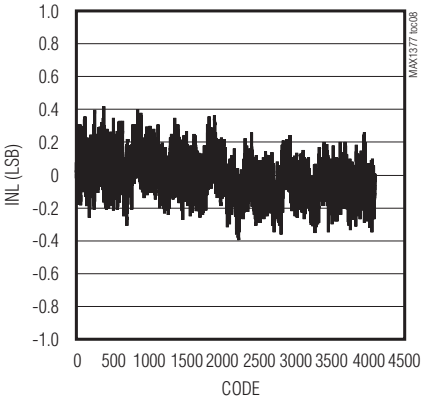
MAX1377 UNIPOLAR FFT



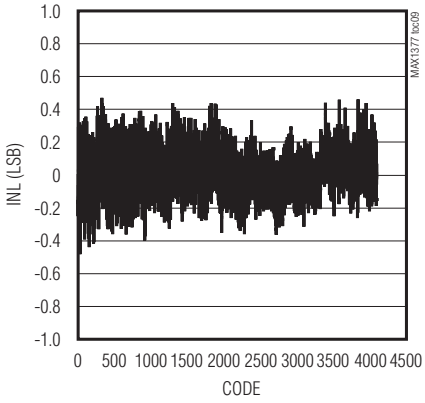
MAX1377 UNIPOLAR DNL vs. OUTPUT CODE



MAX1377 BIPOLAR INL vs. OUTPUT CODE



MAX1377 UNIPOLAR INL vs. OUTPUT CODE

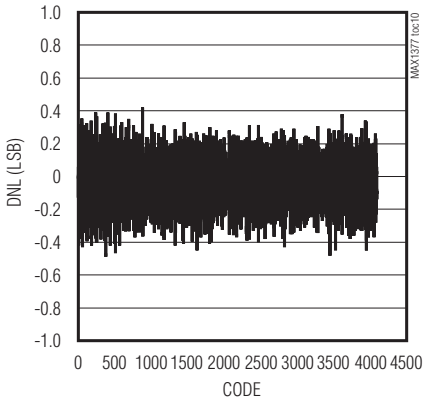


Dual, 12-Bit, 1.25Msps Simultaneous-Sampling ADCs with Serial Interface

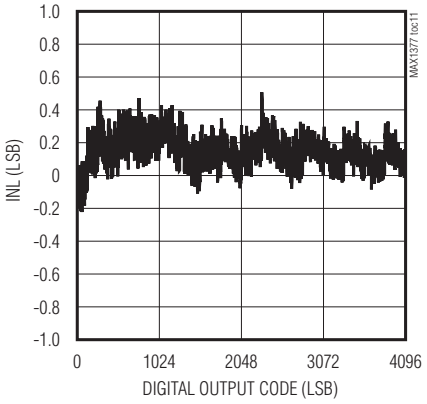
Typical Operating Characteristics (continued)

(V_{AVDD} = 5V/3V, V_L = 3V, f_{SCLK} = 20MHz, T_A = +25°C, unless otherwise noted.)

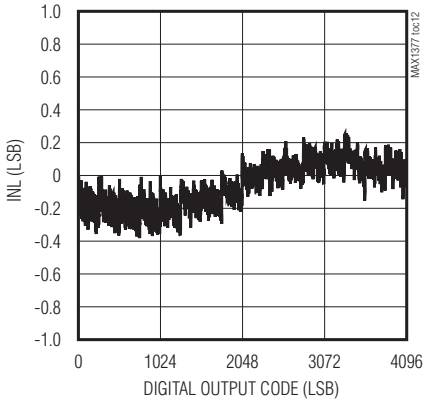
MAX1377 BIPOLAR DNL vs. OUTPUT CODE



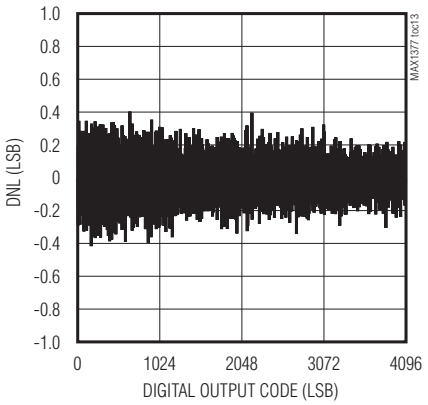
MAX1379 UNIPOLAR INTEGRAL NONLINEARITY vs. DIGITAL OUTPUT CODE



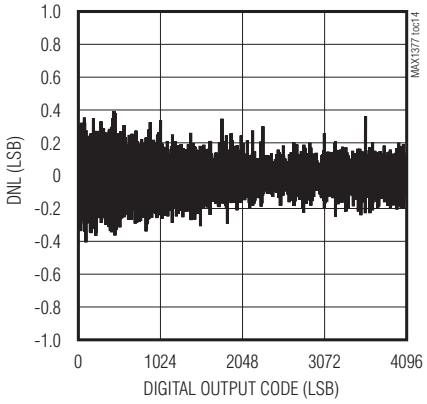
MAX1379 BIPOLAR INTEGRAL NONLINEARITY vs. DIGITAL OUTPUT CODE



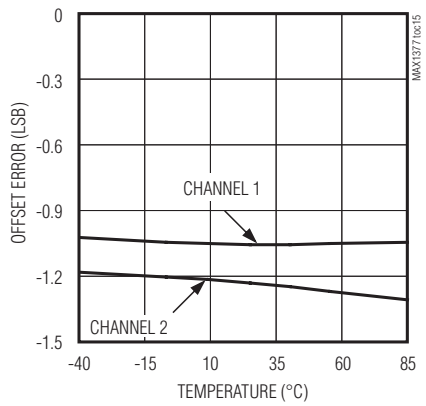
MAX1379 UNIPOLAR DIFFERENTIAL NONLINEARITY vs. DIGITAL OUTPUT CODE



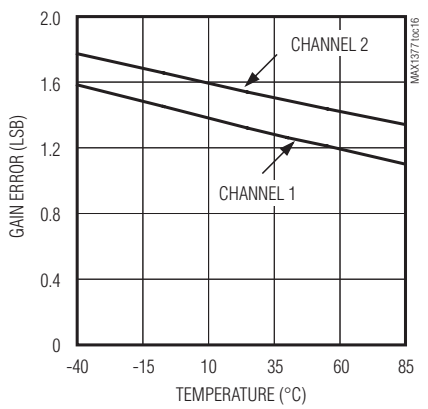
MAX1379 BIPOLAR DIFFERENTIAL NONLINEARITY vs. DIGITAL OUTPUT CODE



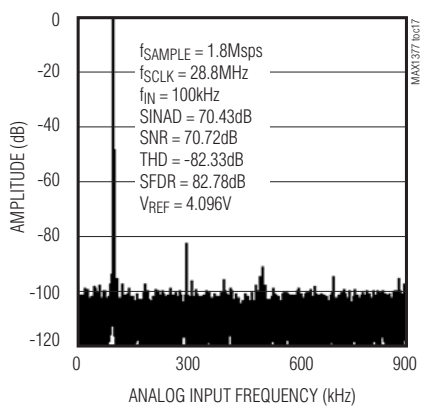
MAX1379 OFFSET ERROR vs. TEMPERATURE



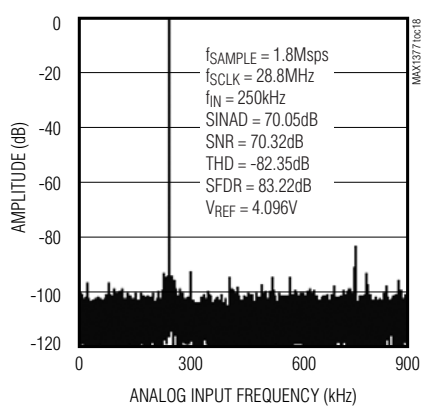
MAX1379 GAIN ERROR vs. TEMPERATURE



MAX1379 FFT PLOT



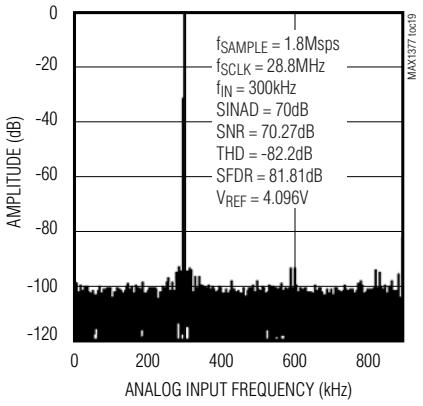
MAX1379 FFT PLOT



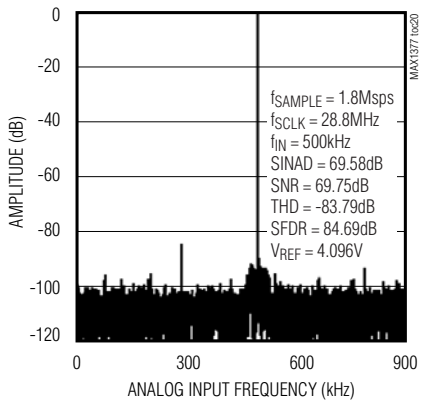
Typical Operating Characteristics (continued)

(V_{AVDD} = 5V/3V, V_L = 3V, f_{SCLK} = 20MHz, T_A = +25°C, unless otherwise noted.)

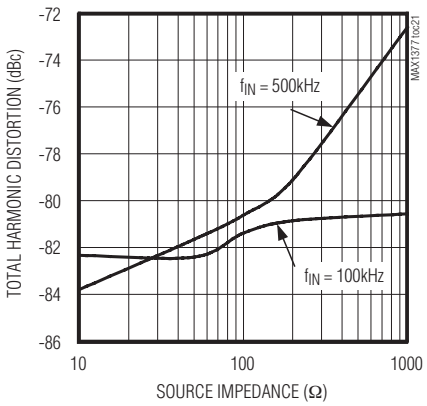
MAX1379 FFT PLOT



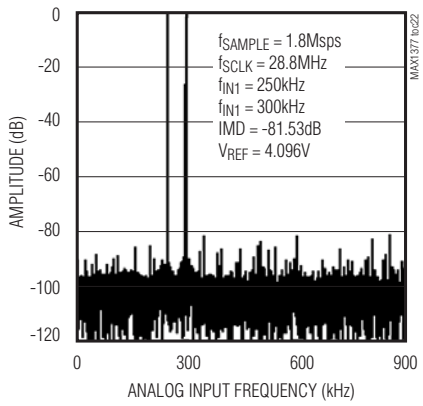
MAX1379 FFT PLOT



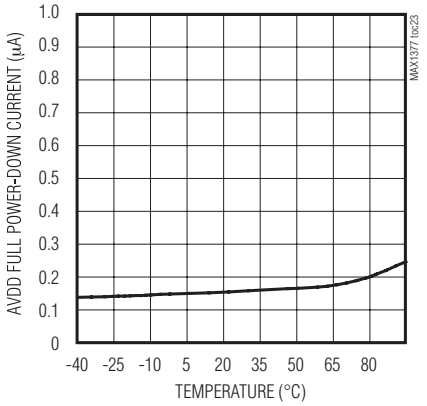
MAX1379 TOTAL HARMONIC DISTORTION vs. SOURCE IMPEDENCE



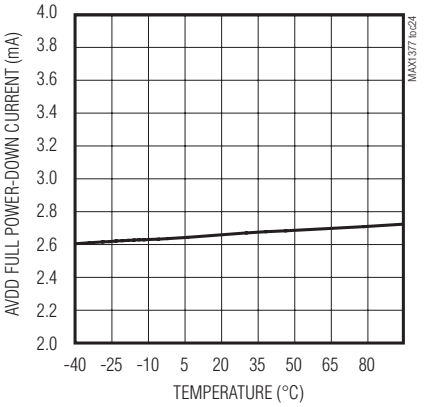
MAX1379 INTERMODULATION PLOT



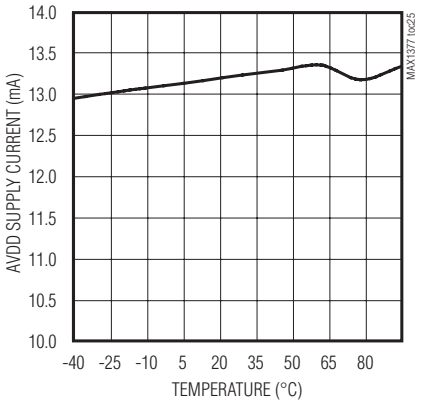
MAX1379 AVDD FULL POWER-DOWN CURRENT vs. TEMPERATURE



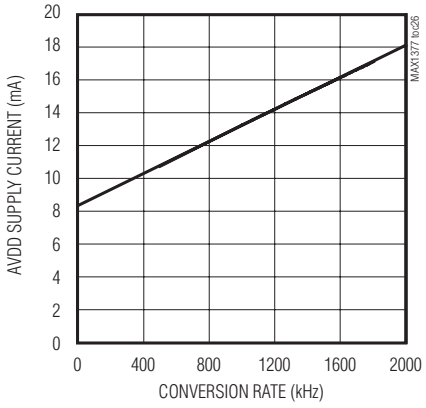
MAX1379 AVDD PARTIAL POWER-DOWN CURRENT vs. TEMPERATURE



MAX1379 AVDD SUPPLY CURRENT vs. TEMPERATURE



MAX1379 AVDD SUPPLY CURRENT vs. CONVERSION RATE

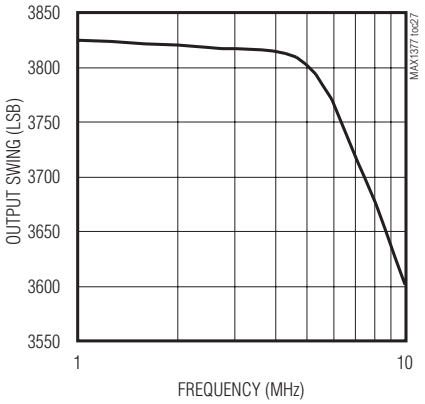


Dual, 12-Bit, 1.25Msps Simultaneous-Sampling ADCs with Serial Interface

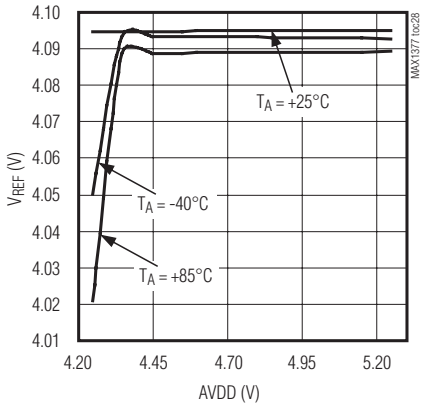
Typical Operating Characteristics (continued)

(V_{AVDD} = 5V/3V, V_L = 3V, f_{SCLK} = 20MHz, T_A = +25°C, unless otherwise noted.)

MAX1379 FULL-SCALE AMPLITUDE vs. FREQUENCY



MAX1379 INTERNAL REFERENCE VOLTAGE vs. ANALOG SUPPLY VOLTAGE



Pin Description

PIN	NAME	FUNCTION
1	REFSEL	Reference-Select Input. Drive REFSEL high to select external reference mode and power down the internal reference. Drive REFSEL low to select internal reference mode.
2	REF	Internal Reference Output/External Reference Input. For internal reference mode, bypass REF to RGND with a ≥ 1µF capacitor. For external reference mode, apply a reference voltage at REF.
3	RGND	Reference Ground/Common Negative Input. In bipolar mode, RGND is the reference ground. In unipolar mode, RGND is the common negative input for all four analog inputs (see Figure 3).
4, 18	AGND	Analog Ground
5	AVDD	Analog-Supply Input. Bypass AVDD with a 10µF ll 10nF capacitor to ground.
6	AIN2A	Primary/Positive Analog Input Channel 2. AIN2A is the primary channel 2 input (AIN2A) if using single-ended inputs ($\overline{U}$/B is low) and the positive channel 2 input (AIN2+) if using differential inputs ($\overline{U}$/B is high) (see Figure 3).
7	AIN2B	Secondary/Negative Analog Input Channel 2. AIN2B is the secondary channel 2 input (AIN2B) if using single-ended inputs ($\overline{U}$/B is low) and the negative channel 2 input (AIN2-) if using differential inputs ($\overline{U}$/B is high) (see Figure 3).
8	$\overline{U}$/B	Unipolar/Bipolar Input. Drive $\overline{U}$/B low to select unipolar mode. Drive $\overline{U}$/B high to select bipolar mode. In bipolar mode, the analog inputs are differential.
9	DGND	Digital Supply Ground
10	V_L	Digital Supply Input. Bypass V_L with a 10µF ll 10nF capacitor to ground.
11	DOUT2	Serial-Data Output 2. Data is clocked out on the rising edge of SCLK.
12	DOUT1	Serial-Data Output 1. Data is clocked out on the rising edge of SCLK.
13	SCLK	Serial-Clock Input. Clocks data out of the serial interface. SCLK also sets the conversion time.
14	CNVST	Conversion-Start Input. Forcing CNVST high prepares the device for a conversion. Conversion begins on the falling edge of CNVST.
15	$\overline{CS}$	Active-Low, Chip-Select Input. Drive $\overline{CS}$ low to enable the serial interface. When $\overline{CS}$ is high, DOUT1 and DOUT2 are high impedance, the serial interface resets, and the device powers down.
16	S/$\overline{D}$	Single-Output/Dual-Output Selection Input. Drive S/$\overline{D}$ high to route ADC2 data through DOUT1 after ADC1 data. Drive S/$\overline{D}$ low for dual outputs with ADC1 data going to DOUT1 and ADC2 data going to DOUT2. See the *Single-/Dual-Output Modes (S/$\overline{D}$)* section.
17	SEL	Analog-Input Selection Input. If $\overline{U}$/B is low (unipolar mode), drive SEL low to select the primary inputs, AIN1A and AIN2A. Drive SEL high to select the secondary inputs, AIN1B and AIN2B. In bipolar mode, SEL is ignored.
19	AIN1B	Secondary/Negative Analog Input Channel 1. AIN1B is the secondary channel 1 input (AIN1B) if using single-ended inputs ($\overline{U}$/B is low) and the negative channel 1 input (AIN1-) if using differential inputs ($\overline{U}$/B is high) (see Figure 3).
20	AIN1A	Primary/Positive Analog Input Channel 1. AIN1A is the primary channel 1 input (AIN1A) if using single-ended inputs ($\overline{U}$/B is low) and the positive channel 1 input (AIN1+) if using differential inputs ($\overline{U}$/B is high) (see Figure 3).
—	EP	Exposed Pad. EP is internally connected to AGND.

Dual, 12-Bit, 1.25Msps Simultaneous-Sampling ADCs with Serial Interface

Detailed Description

The MAX1377/MAX1379/MAX1383 use an input track and hold (T/H) and SAR circuitry to convert an analog input signal to a digital 12-bit output. The dual serial interface requires a minimum of three digital lines (SCLK, CNVST, and DOUT) and provides easy interfacing to microprocessors (µPs) and DSPs. Four digital lines are required for dual-output mode.

Input T/H Circuit

Upon power-up, the input T/H circuit enters its tracking mode immediately. Following a conversion, the T/H enters the tracking mode on the 14th SCLK rising edge of the previous conversion (Figure 6). The T/H enters the hold mode on the falling edge of CNVST. The time required for the T/H to acquire an input signal is determined by how quickly the input capacitance is charged. If the input signal's source impedance is high, the acquisition time lengthens. The acquisition time, t_{ACQ}, is the minimum time needed for the signal to be acquired (see the *Definitions* section). t_{ACQ} is calculated by the following equation:

$$t_{ACQ} \geq 9 \times (R_S + R_{IN}) \times C_{IN}$$

where R_{IN} = 450Ω, C_{IN} = 16pF, and R_S is the source impedance of the input signal.

Figure 1 shows the acquisition time as tested using the circuit of Figure 2. The acquisition time is the time between the rising edge of a 1V to 3V step input and the falling edge of CONVST which produced a stable sample. Rs represents the source impedance of the function generator (50Ω) and Rx represents the variable filter resistance.

Unipolar Mode

The MAX1377/MAX1379/MAX1383 support two simultaneously sampled, single-ended conversions in unipolar mode. Drive $\overline{U}$/B low for unipolar mode. In unipolar mode, switches A–D in Figure 3 close according to the position of SEL. Drive SEL low to close switches A and D and designate AIN1A and AIN2A as the active, single-ended inputs referenced to RGND. Drive SEL high to close switches B and D and select AIN1B and AIN2B as the active, single-ended inputs referenced to RGND. The output code in unipolar mode is straight binary. See Figure 4 for the unipolar transfer function.

Bipolar Mode

Drive $\overline{U}$/B high to configure the inputs for bipolar/differential mode. Switches A and C in Figure 3 are closed, designating AIN1A (AIN2A) and AIN1B (AIN2B) as the active, differential inputs. In bipolar mode, SEL is ignored. The output code is in two's complement. Figure 5 shows the transfer function for bipolar mode.

Input Bandwidth

The ADC's input-tracking circuitry has a 5MHz small-signal bandwidth, allowing the ADC to digitize high-speed transient events and measure periodic signals with bandwidths exceeding the ADC's sampling rate by using undersampling techniques. To avoid high-frequency signals being aliased into the frequency band of interest, anti-alias filtering is recommended.

Analog Input Protection

Internal protection diodes that clamp the analog input to AVDD and AGND allow the analog inputs to swing from AGND - 0.3V to AVDD + 0.3V without damage to

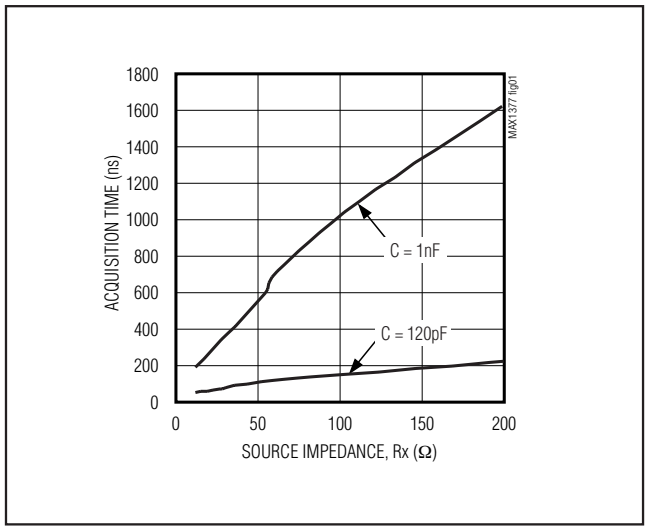


Figure 1. Acquisition Time vs. Source Impedance

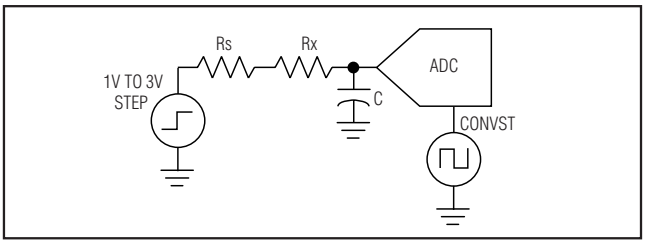


Figure 2. Test Circuit

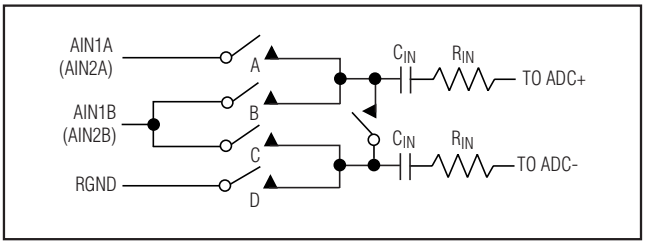


Figure 3. Equivalent Input Circuit

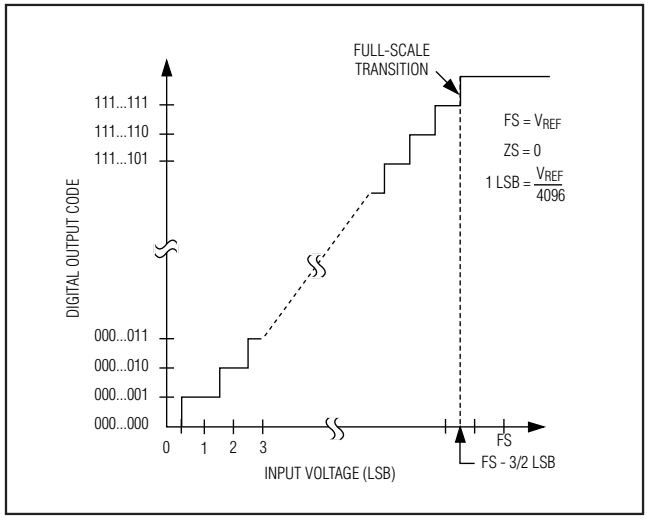


Figure 4. Unipolar Transfer Function ($\overline{U}$/B = Low)

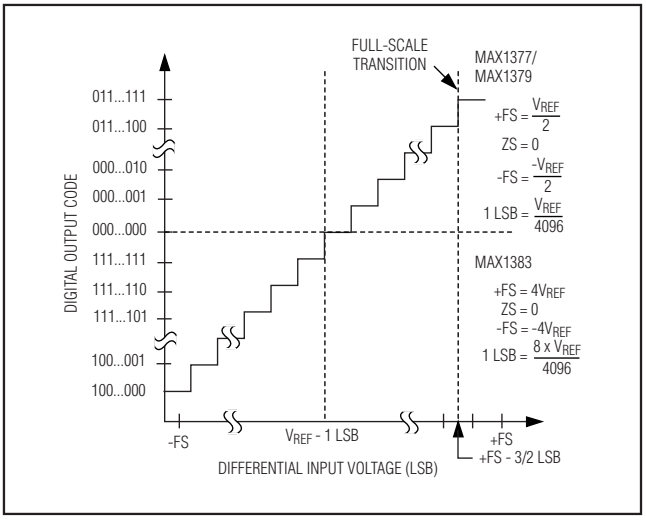


Figure 5. Bipolar Transfer Function ($\overline{U}$/B = High)

the MAX1377 and MAX1379. The MAX1383 can handle ±10V input swings. All inputs must not exceed the stated ranges for accurate conversions.

Internal Reference Mode

Drive REFSEL low to select internal reference mode. The MAX1377 includes an on-chip 2.048V reference; the MAX1379 has a 4.096V reference; and the MAX1383 includes a 2.5V internal reference. The reference output at REF can be used as a reference voltage source for other components. REF can source up to 2mA. Bypass REF with a 10nF capacitor and a 4.7µF capacitor to RGND. It is important to select a low ESR capacitor and keep the trace resistance as low as possible.

The internal reference is continuously powered-up during both normal and partial power-down modes. In full power-down mode, the internal reference is disabled. Allow at least 2ms recovery time after a power-on reset or exiting full power-down mode for the reference to settle to its intended value.

Input Voltage Range (MAX1383)

The input range on the MAX1383 has an 8x relationship with the reference voltage. For example, when the reference voltage (internal or external) is 2.5V, the input range is ±10V ($20V_{P-P}$).

External Reference Mode

Drive REFSEL high to select external reference mode. Apply a reference voltage at REF. Bypass REF with a 10nF capacitor and a 4.7µF capacitor to RGND. As with the internal reference, it is important to select a low ESR capacitor and keep the trace resistance as low as possible.

Serial Interface

Initialization After Power-Up

Upon initial power-up, the MAX1377/MAX1379/ MAX1383 require a complete conversion cycle to initialize the internal calibration. Following this initialization, the ADC is ready for normal operation. This initialization is only required after a hardware power-on reset and is not required after exiting partial or full power-down mode.

Starting a Conversion and Reading the Output

With SCLK idling high or low, a falling edge on CNVST begins a conversion (see Figure 6). This causes the analog input stage to transition from track to hold mode. SCLK provides the timing for the conversion process, and data is shifted out as each bit of the result is determined. A rising edge in CNVST forces the device into one of three modes. The mode is determined by the clock cycle in which the transition occurs and whether the device is set for single or dual outputs. Figures 7 and 8 show each mode that is activated with a rising CNVST edge for single and dual outputs.

DOUT1 (and DOUT2, if S/$\overline{D}$ = low) transitions from high impedance to being actively driven low once the ADC enters hold mode. DOUT_ remains low for the first three SCLK pulses and begins outputting the conversion result after the 4th rising edge of SCLK, MSB first. DOUT_ transitions complete t_{DOUT} after each SCLK rising edge and the DOUT_ values remain valid for t_{HOLD} after the next rising edge of SCLK. A total of 16 SCLK pulses are required to complete a normal conversion in dual-output mode and 28 SCLK pulses in single-output mode. DOUT_ goes low after the 16th rising edge of SCLK and goes high-impedance when CNVST goes high.

Dual, 12-Bit, 1.25Msps Simultaneous-Sampling ADCs with Serial Interface

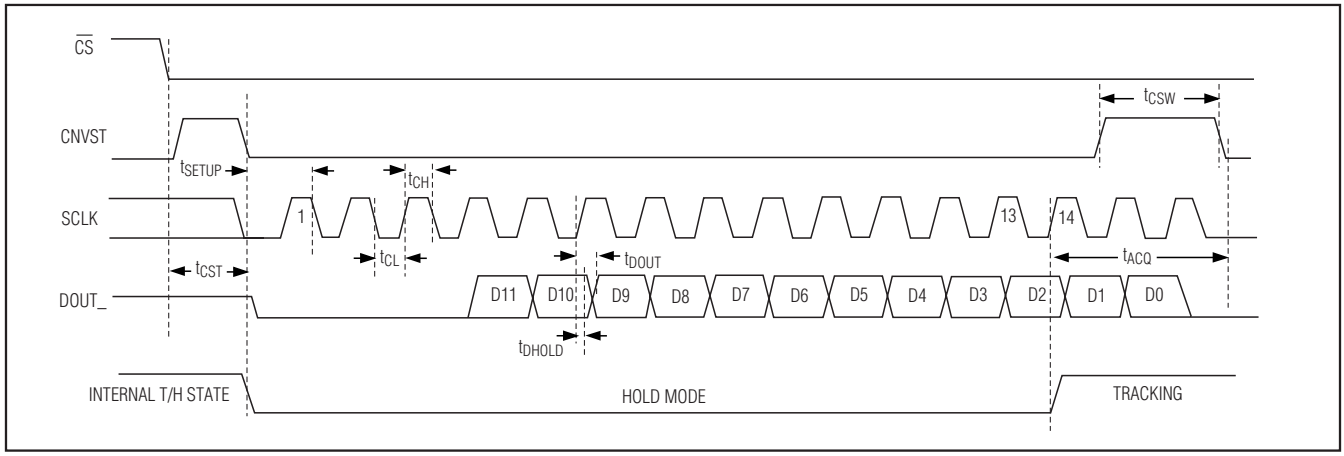


Figure 6. Detailed Serial-Interface Timing Diagram

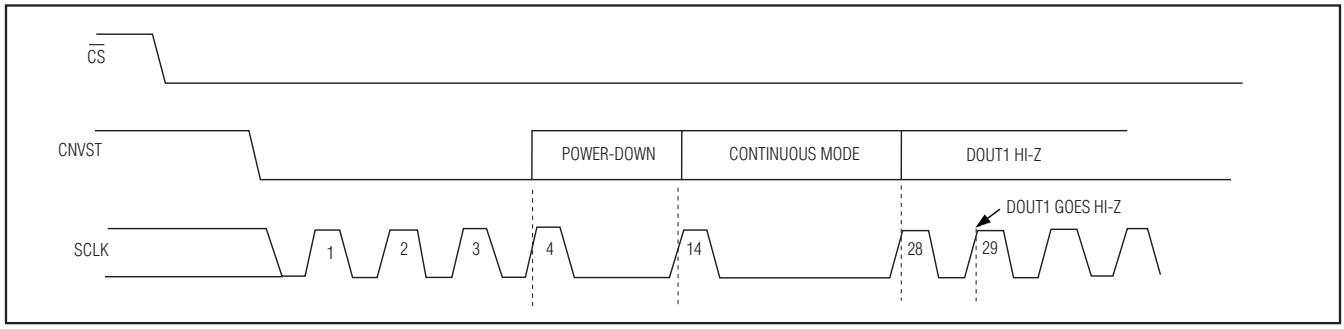


Figure 7. Single-Output CNVST Transition Modes

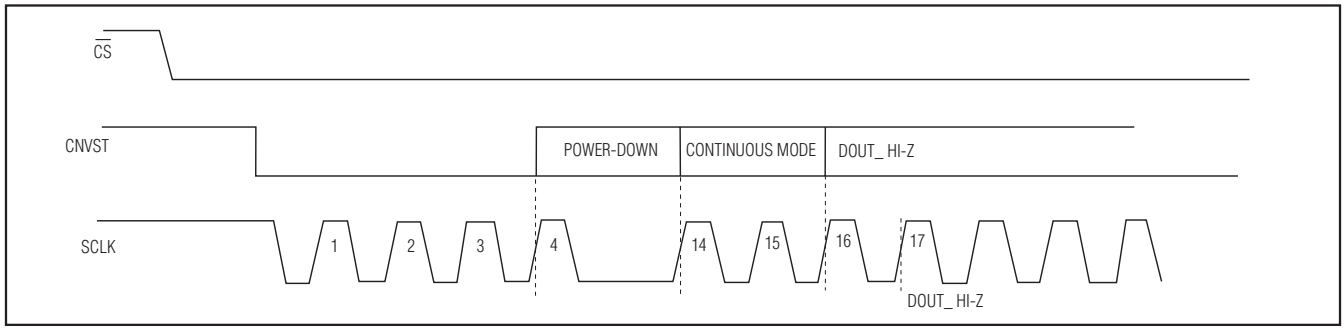


Figure 8. Dual-Output CNVST Transition Modes

For continuous operation in single-output mode, pull CNVST high after the 14th rising and before the 28th rising edge of SCLK. In dual-output mode, if CNVST returns high after the 14th rising and before the 16th falling edge of SCLK, DOUT_ remains active so continuous conversions can be sustained. If CNVST is low during the 16th edge of SCLK (dual-conversion mode) and the 28th falling edge of SCLK (single-output mode), DOUT_ returns to its high-impedance state on the next rising edge of CNVST or SCLK, enabling the serial interface to be shared by multiple devices. See Figures 9 and 10 for single and continuous conversion timing diagrams.

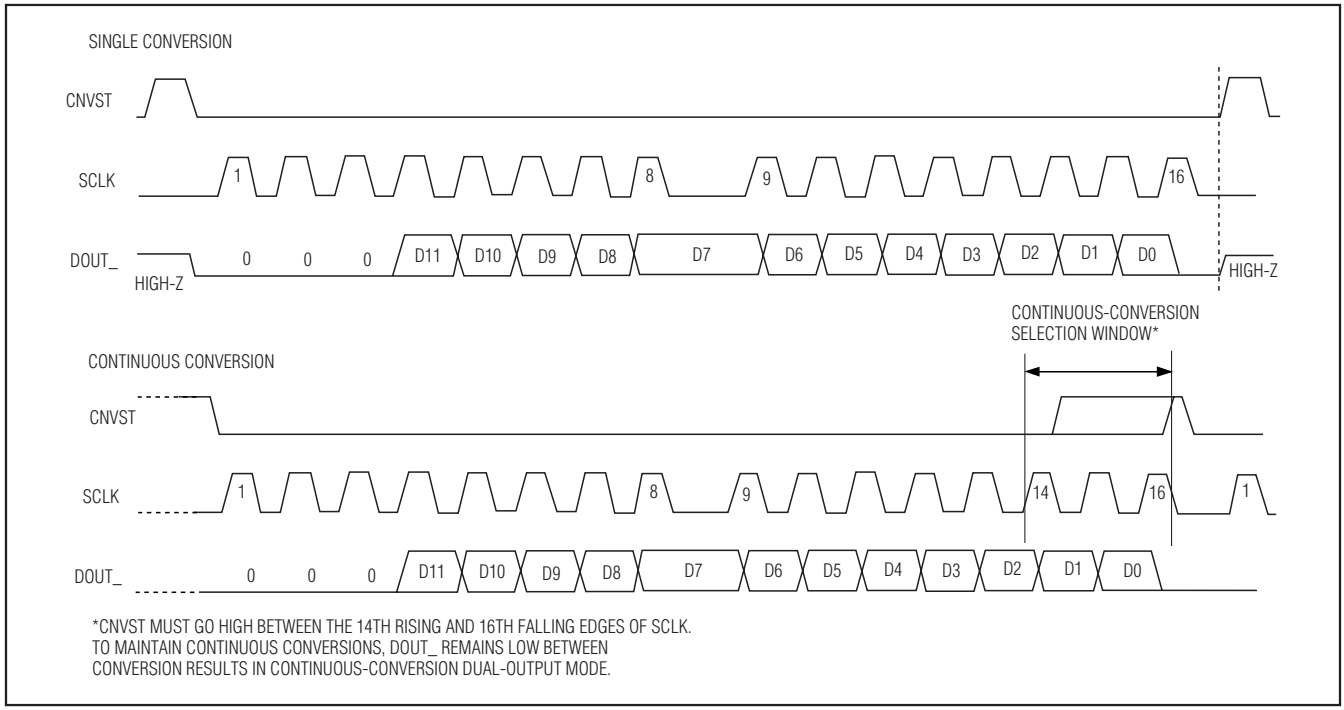


Figure 9. Dual-Output Mode, Single and Continuous Conversions

Single-/Dual-Output Modes (S/$\overline{D}$)

In dual-output mode, conversion results from the two channels appear on separate outputs. DOUT1 outputs the result from channel 1 and DOUT2 outputs the result from channel 2. Drive S/$\overline{D}$ low to operate in dual-output mode. For DSPs with two-buffer and two-input-stream capability, use the dual-output mode to allow for easier DSP software for dual streams. Two buffer locations can be used so the streams do not need to be separated.

In single-output mode, the results from both channels appear on DOUT1. The channel 2 conversion result follows the channel 1 conversion result (see Figure 10). The MSB (D11) of the channel 2 conversion result appears on DOUT1 after the 16th rising edge of SCLK. The LSB (D0) of the channel 2 conversion result appears on DOUT1 after the 27th rising edge of SCLK and is ready to be clocked in on the 28th rising edge of SCLK. DOUT2 is high-impedance when S/$\overline{D}$ is high.

If CNVST goes high after the 28th rising edge of SCLK, DOUT1 goes high impedance until the next conversion is initiated (single-conversion mode). If CNVST goes high after the 14th rising edge and before the 28th rising edge of SCLK, DOUT1 is actively driven low until the next conversion results are ready (continuous- conversion mode).

Note: In single-output mode, the conversion speed is limited to 0.625Msps by the maximum SCLK.

Power-Down Modes

Partial Power-Down (PPD)

Reduce power consumption by placing the MAX1377/MAX1379/MAX1383 in partial or full power-down mode. Partial power-down mode is ideal for infrequent data sampling and applications requiring fast wake-up times. Pull CNVST high after the 3rd and before the 14th rising edge of SCLK to place the device in partial power-down mode. This reduces the analog supply current to 2mA. While in partial power-down mode, the internal reference remains enabled (if REFSEL = GND). Figure 11 shows the timing sequence to enter partial power-down mode.

Full Power-Down Mode (FPD)

Full power-down mode is ideal for infrequent data sampling and very low-supply current applications. To enter full power-down mode, place the MAX1377/MAX1379/MAX1383 first in partial power-down mode. Perform the

Dual, 12-Bit, 1.25Msps Simultaneous-Sampling ADCs with Serial Interface

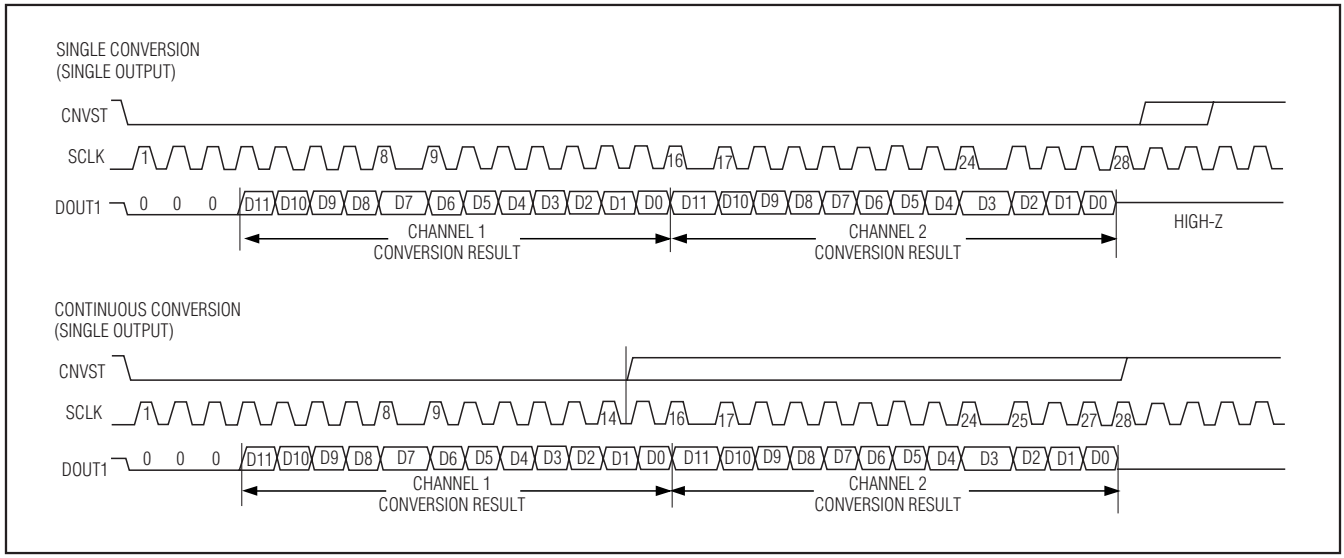


Figure 10. Single-Output Mode, Single and Continuous Conversions

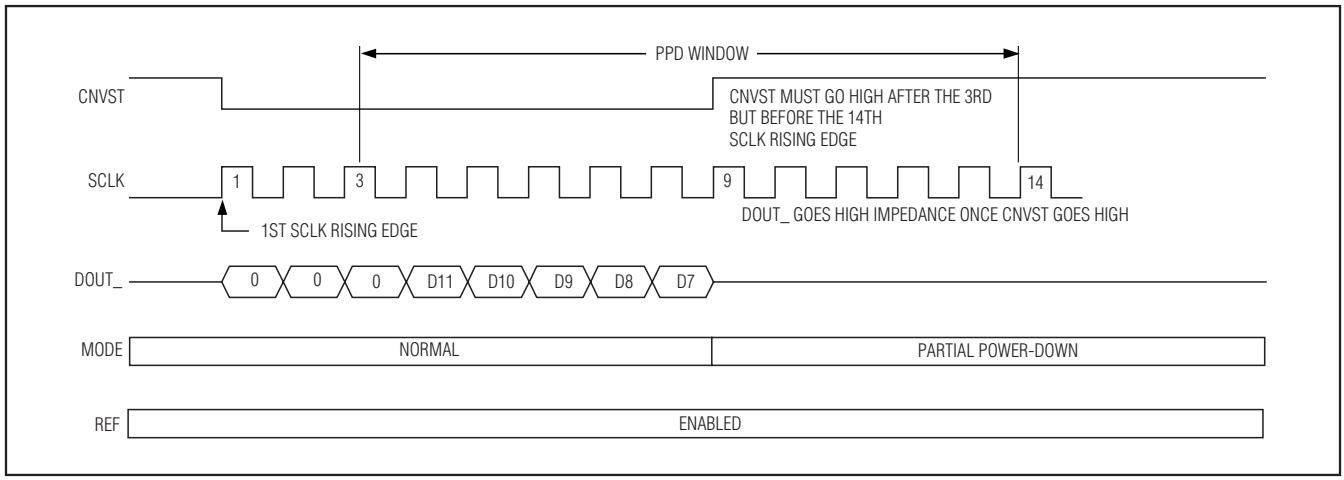


Figure 11. Partial Power-Down Timing Sequence

CNVST/SCLK sequence necessary to enter partial power-down mode. Repeat the same sequence to enter full power-down mode. In full power-down mode, the internal reference is disabled to minimize power consumption. Figure 12 shows the timing sequence to enter full power-down mode.

Another way to enter the full power-down mode is to drive $\overline{CS}$ high. If $\overline{CS}$ is high, the MAX1377/MAX1379/MAX1383 act as if the full power-down sequence were issued. To exit the $\overline{CS}$-initiated power-down mode, drive $\overline{CS}$ low. Allow 2ms for the reference to wake up and settle before performing a conversion.

Exiting Partial and Full Power-Down Modes

Drive CNVST low and allow at least 14 SCLK cycles to elapse before driving CNVST high to exit partial or full power-down mode. When exiting partial power-down mode, conversions can begin immediately without having to wait for the reference to wake-up. When exiting full power-down mode, allow at least 2ms recovery time after exiting to ensure that the internal reference has settled.

In partial or full power-down mode, maintain idle SCLK low or high to minimize power.

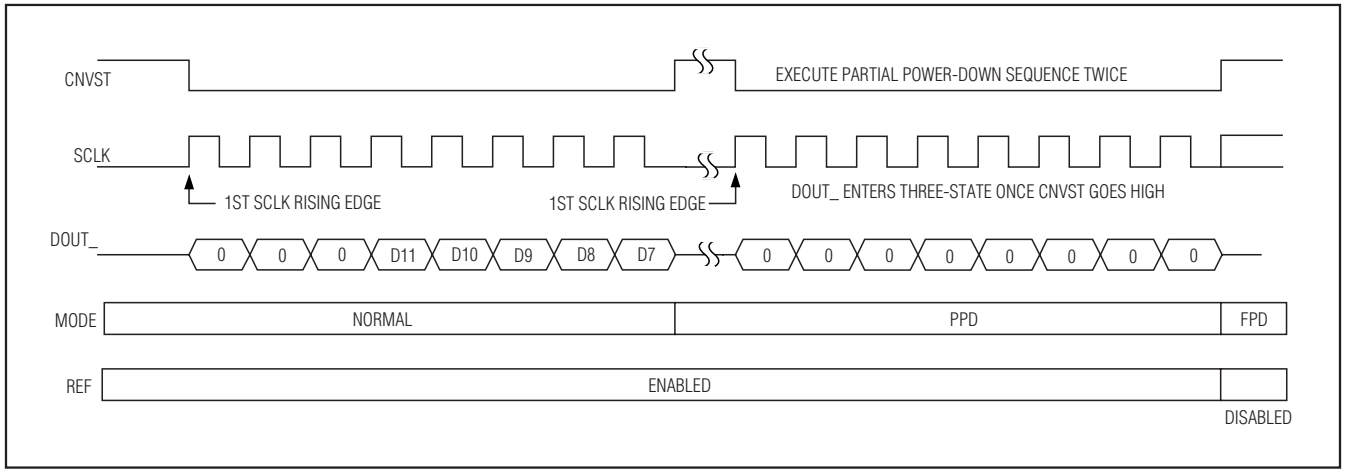


Figure 12. Full Power-Down Mode Timing Sequence

Applications Information

SPI and MICROWIRE

The MAX1377/MAX1379/MAX1383 are compatible with all four modes programmed with the CPHA and CPOL bits in the SPI or MICROWIRE control register. Conversion begins with a CNVST falling edge. DOUT_ goes low, indicating a conversion is in progress. Two consecutive 8-bit reads are required to get the full 12 bits from the ADC. DOUT_ transitions on the rising edge of SCLK. DOUT_ is guaranteed to be valid t_{DOUT} after the rising edge of SCLK and remains valid until t_{DHOLD} after the next SCLK rising edge (see Figure 13).

For CPOL = 0 and CPHA = 0 or CPOL = 1 and CPHA = 1, the data is clocked into the µC on the rising edge of SCLK. For CPOL = 0 and CPHA = 1 or CPOL = 1 and CPHA = 0, the data is clocked into the µC on the falling edge of SCLK. The MAX1377/MAX1379/MAX1383 are compatible with all CPOL/CPHA configurations since the data is valid on the falling and rising edge of SCLK.

QSPI

Unlike SPI, which requires two 8-bit reads to acquire the 12 bits of data from the ADC, QSPI allows the minimum number of clock cycles necessary to clock in the data. The MAX1377/MAX1379/MAX1383 require 16 clock cycles from the µC to clock out the 12 bits of data. The conversion result contains three zeros followed by the 12 data bits, and a trailing zero with the data in the MSB-first format.

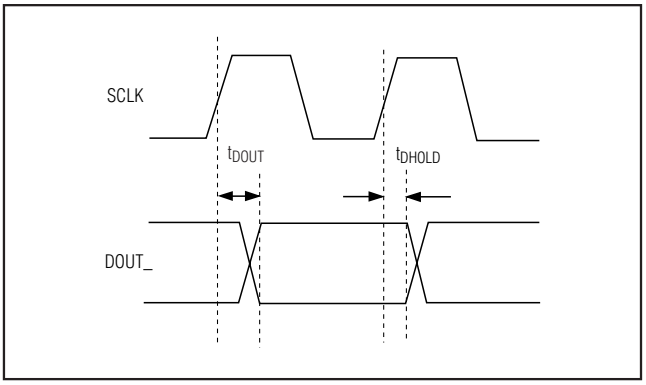


Figure 13. Data Valid and Hold Times

Three-Phase Motor Controller

The MAX1377/MAX1379/MAX1383 are ideally suited for motor-control systems (Figure 16). The devices' simultaneously sampled inputs eliminate the need for complicated DSP algorithms that realign sequentially sampled data into a simultaneous sample set. The ±10V (MAX1383) input allows for standard industrial inputs, eliminating the need for voltage-scaling amplifiers.

Wireless Communication

Use the MAX1377/MAX1379/MAX1383 in a variety of wireless communication systems. These devices allow precise, simultaneous sampling of the I and Q signals of quadrature RF receiver systems. Figure 17 shows the MAX1377 in a simplified quadrature system. The device has a differential input option that allows either full differential or psuedo-differential signals. The 2:1 input mux allows measurement of RSSI and other system-monitoring functions with this device.

Dual, 12-Bit, 1.25Msps Simultaneous-Sampling ADCs with Serial Interface

Layout, Grounding, and Bypassing

For best performance, use PCBs with ground planes. Ensure that digital and analog signal lines are separated from each other. Do not run analog and digital (especially clock) lines parallel to one another or digital lines underneath the ADC package.

Establish a single-point analog ground (star ground point) at AGND, separate from the digital ground, DGND. Connect all other analog grounds and DGND to this star ground point for further noise reduction. The ground return to the power supply for this ground should be low impedance and as short as possible for noise-free operation. See Figure 14.

High-frequency noise in the AVDD power supply affects the ADC's high-speed comparator. Bypass the supply to the single-point analog ground with 0.01µF and 10µF bypass capacitors. Minimize capacitor lead lengths for best supply-noise rejection.

Definitions

Integral Nonlinearity

Integral nonlinearity (INL) is the deviation of the values on an actual transfer function from a straight line. This straight line can be either a best-straight-line fit or a line drawn between the end points of the transfer function, once offset and gain errors have been nulled. The static linearity parameters for the MAX1377/MAX1379/MAX1383 are measured using the end-points method.

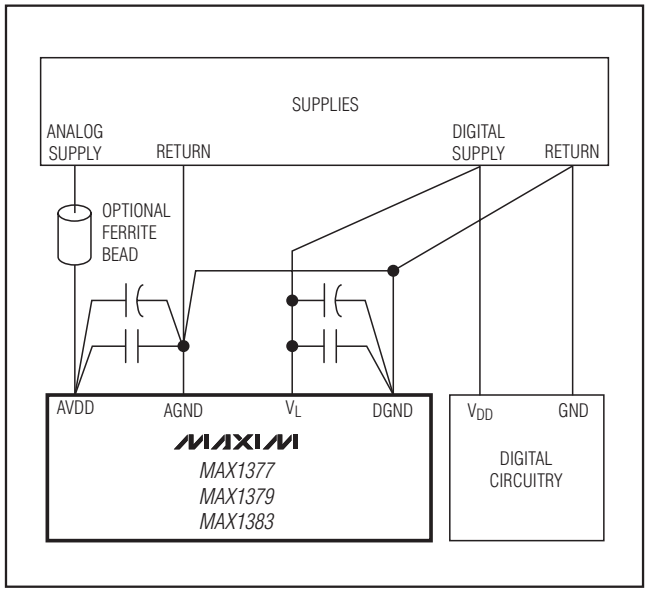


Figure 14. Power-Supply Grounding and Bypassing

Differential Nonlinearity

Differential nonlinearity (DNL) is the difference between an actual step width and the ideal value of 1 LSB. A DNL error specification of 1 LSB or less guarantees no missing codes and a monotonic transfer function.

Aperture Jitter

Aperture jitter (t_{AJ}) is the sample-to-sample variation in the time between the samples.

Aperture Delay

Aperture delay (t_{AD}) is the time defined between the falling edge of CNVST and the instant when an actual sample is taken.

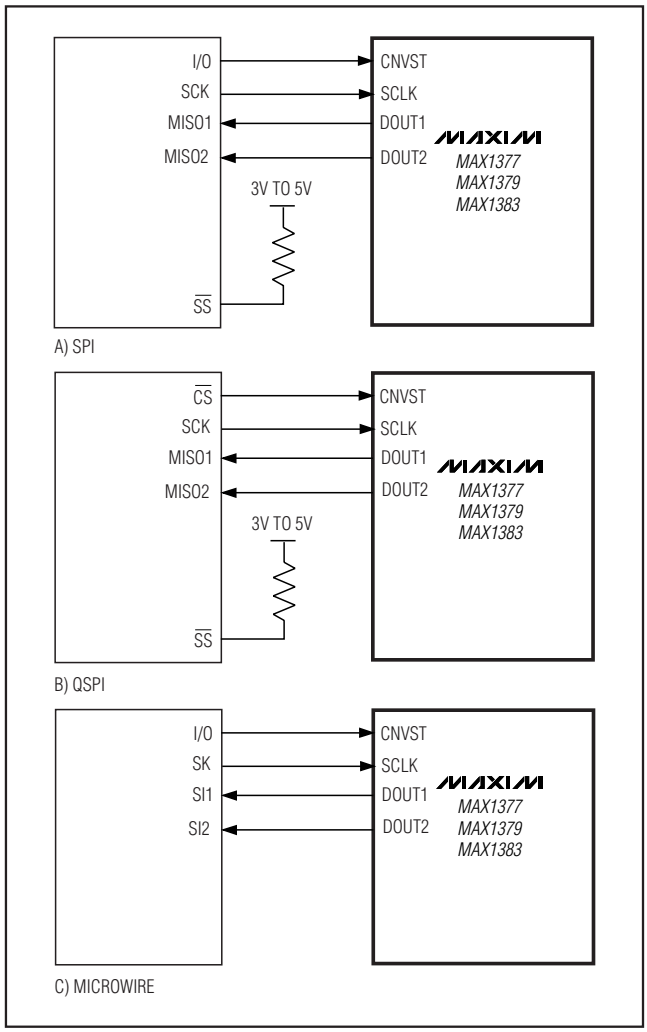


Figure 15. Common Serial-Interface Connections to the MAX1377/MAX1379/MAX1383

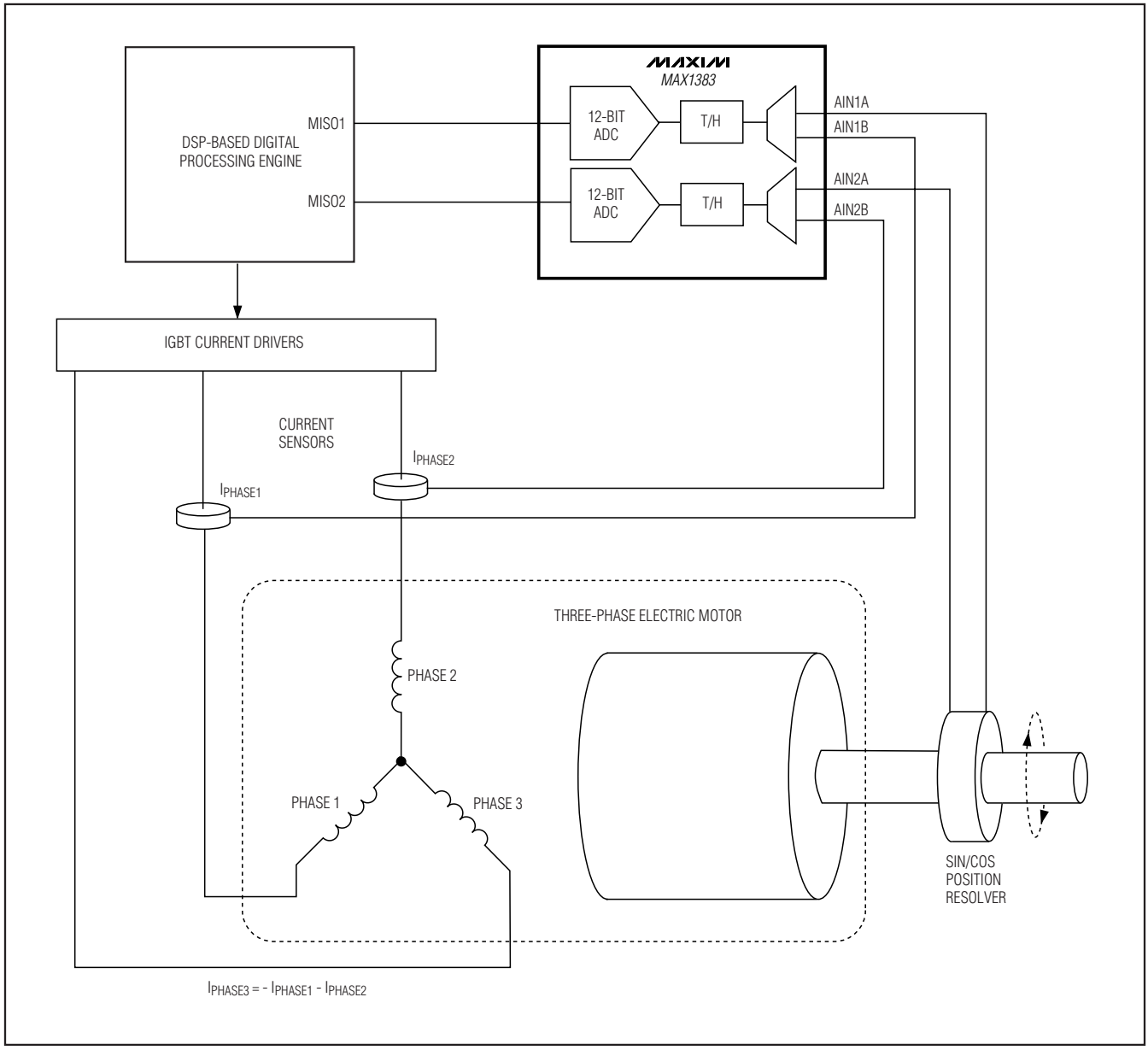


Figure 16. Three-Phase Motor Control

Dual, 12-Bit, 1.25Msps Simultaneous-Sampling ADCs with Serial Interface

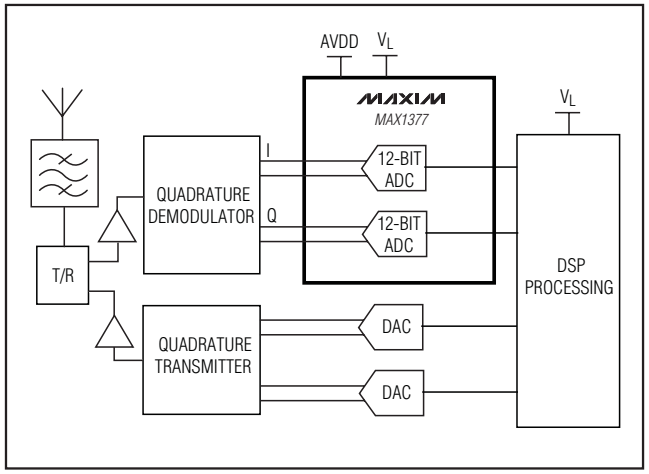


Figure 17. Quadrature Wireless-Communication System

Signal-to-Noise Ratio

For a waveform perfectly reconstructed from digital samples, signal-to-noise ratio (SNR) is the ratio of full-scale analog input (RMS value) to the RMS quantization error (residual error). The theoretical minimum analog-to-digital noise is caused by quantization error, and results directly from the ADC's resolution (N bits):

$$SNR = (6.02 \times N + 1.76)dB$$

In reality, there are other noise sources besides quantization noise, including thermal noise, reference noise, clock jitter, etc. Therefore, SNR is computed by taking the ratio of the RMS signal to the RMS noise, which includes all spectral components minus the fundamental, the first five harmonics, and the DC offset.

Signal-to-Noise Plus Distortion

Signal-to-noise plus distortion (SINAD) is the ratio of the fundamental input frequency's RMS amplitude to the RMS equivalent of all other ADC output signals:

$$SINAD(dB) = 20 \times \log(SignalRMS/NoiseRMS)$$

Effective Number of Bits

Effective number of bits (ENOB) indicates the global accuracy of an ADC at a specific input frequency and sampling rate. An ideal ADC's error consists of quantization noise only. With an input range equal to the full-scale range of the ADC, calculate the ENOB as follows:

$$ENOB = \left(\frac{SINAD - 1.76}{6.02}\right)$$

Total Harmonic Distortion

Total harmonic distortion (THD) is the ratio of the RMS sum of the first five harmonics of the input signal to the fundamental itself. This is expressed as:

$$THD = 20 \times \log\left(\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2}}{V_1}\right)$$

where V_1 is the fundamental amplitude, and V_2 through V_5 are the amplitudes of the 2nd- through 5th-order harmonics.

Spurious-Free Dynamic Range

Spurious-free dynamic range (SFDR) is the ratio of the RMS amplitude of the fundamental (maximum signal component) to the RMS value of the next largest distortion component.

Full-Power Bandwidth

Full-power bandwidth is the frequency at which the input signal amplitude attenuates by 3dB for a full-scale input.

Full-Linear Bandwidth

Full-linear bandwidth is the frequency at which the signal-to-noise plus distortion (SINAD) is equal to 56dB.

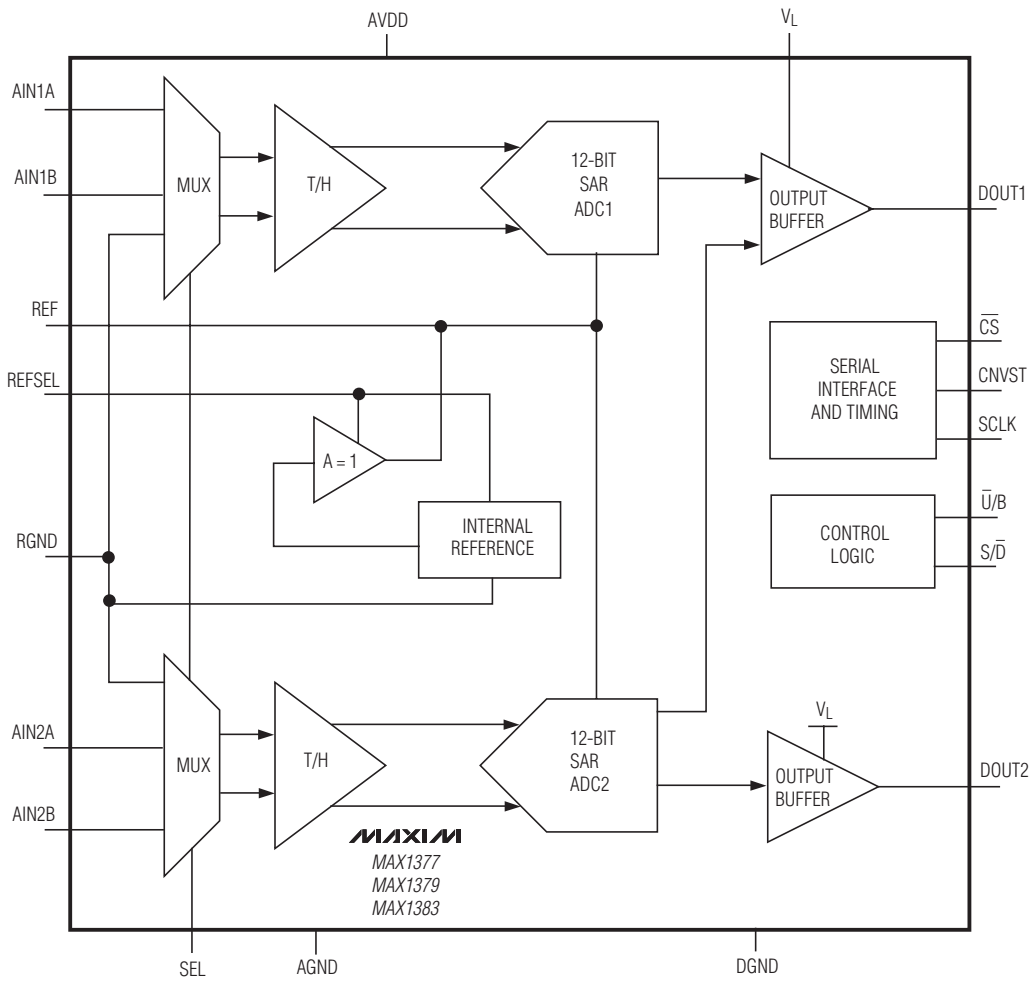
Intermodulation Distortion

Any device with nonlinearities creates distortion products when two sine waves at two different frequencies (f1 and f2) are input into the device. Intermodulation distortion (IMD) is the total power of the IM2 to IM5 intermodulation products to the Nyquist frequency relative to the total input power of the two input tones, f1 and f2. The individual input tone levels are at -6dBFS.

Chip Information

PROCESS: BiCMOS

Functional Diagram



Selector Guide

PART	SUPPLY VOLTAGE (V)	INTERNAL REFERENCE VOLTAGE (V)	INPUT VOLTAGE RANGE	SAMPLING RATE (Msps)
MAX1377	2.7 to 3.6	2.048	0 to V_{REF}, $\pm V_{REF}/2$	1.25
MAX1379	4.75 to 5.25	4.096	0 to V_{REF}, $\pm V_{REF}/2$	1.25
MAX1383	4.75 to 5.25	2.5	±10V	1.25

Dual, 12-Bit, 1.25Msps Simultaneous-Sampling ADCs with Serial Interface

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
20 TQFN-EP	T2055-4	**21-0140**